IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:	Douglas Piasecki, Ka Leung and Ken Fernald
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Group:	2819
Examiner:	Linh V. Nguyen
For:	METHOD AND APPARATUS FOR SUBCLOCKING A SAR ANALOG-TO-DIGITAL CONVERTER

Mail Stop Issue Fee
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

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AMENDMENT UNDER RULE 312

The above-identified application has been carefully reviewed prior to the payment of the issue fee. It is requested that the following amendments be entered under the provisions of Rule 312.

1. (Previously Presented): A method for clocking the operation of a SAR analog-to-digital converter (ADC), comprising the steps of:

providing a low frequency clock and a high frequency clock;

tracking an analog input voltage during a tracking phase to sample the value thereof;

initiating a conversion cycle referenced to an edge of the low frequency clock;

converting the sampled data in a conversion operation during a data conversion cycle, which conversion operation requires a plurality of conversion clock cycles; and

controlling the timing of at least a portion of the conversion operation during the data conversion cycle utilizing the high frequency clock as the conversion clock.

2. (Previously Presented): The method of Claim 1, wherein the step of controlling the at least a portion of the conversion operation comprises utilizing the high frequency clock during the conversion cycle to control the timing of the at least a portion of the conversion operation proximate in time to the step of initiating.

3. (Previously Presented): The method of Claim 1, wherein the at least a portion of the conversion operation comprises substantially all of the conversion operation.

4. (Previously Presented): The method of Claim 1, wherein the SAR ADC has an n-bit resolution and the conversion operation includes the steps of:

testing each of the n-bits during the conversion operation to determine the logic state thereof, the timing thereof determined by a conversion clock that generates the conversion clock cycles;

generating the conversion clock from the low frequency clock during the tracking phase; and

during the step of controlling, generating the conversion clock from the high frequency clock for the at least a portion of the conversion operation.

5. (Previously Presented): The method of Claim 4, wherein the step of generating the conversion clock comprises generating the conversion clock substantially only during the at least a portion of the conversion operation.

6. (Previously Presented): The method of Claim 4, wherein the at least a portion of the conversion operation does not include the time to test all of the n-bits.

7. (Previously Presented): The method of Claim 4, wherein the at least a portion of the conversion operation includes the time to test substantially all of the n-bits.

8. (Previously Presented): The method of Claim 4, wherein the at least a portion includes all of the n-bits.

9. (Previously Presented): The method of Claim 1, wherein the step of initiating is in response to the generation of a convert initiation signal generated by a processing unit.

10. (Previously Presented): The method of Claim 9, wherein the processing unit operates from the low frequency clock and, during the step of controlling the timing of at least a portion of the conversion operation, the processing unit continues to operate on the low frequency clock.

11. (Previously Presented): The method of Claim 1, wherein the SAR ADC operates in a power up mode and in a power down mode, when in the power down mode, further comprising the steps of:

operating the SAR ADC in a low power mode;

receiving a power up signal and, in response thereto:

applying power to the SAR ADC,

initiating the tracking operation,

delaying the start of the conversion cycle by a predetermined delay to allow the SAR ADC to stabilize, and

after the end of the conversion cycle, removing power to the SAR ADC.

12. (Previously Presented): The method of Claim 11, and further comprising the step of introducing a known programmable amount of delay to force the tracking operation to continue for that programmable amount of delay and delaying the start of the conversion cycle for the programmable amount of delay.

13. (Previously Presented): A method for operating a SAR ADC in a mixed signal processing system, comprising the steps of:

operating a digital processing section on a first and low frequency clock;

generating a convert request to instruct the SAR ADC to initiate a conversion operation;

in response to the generation of the convert request, operating the SAR ADC in a data conversion operation on a second and high frequency clock that has a clock frequency that is higher than the frequency of the low frequency clock to convert an analog value on an analog input to a digital value in a SAR conversion cycle;

storing the resultant digital value for processing by the digital processing section; and

after storage of the resultant digital value, processing the resultant digital value by the digital processing section.

14. (Previously Presented): The method of Claim 13, wherein the conversion operation is completed within at least a single cycle of the low frequency clock.

15. (Previously Presented): The method of Claim 13, wherein:

the step of operating the SAR ADC in a data conversion operation comprises, in response to the generation of the convert request, operating the SAR ADC in a plurality of data

conversion operations on the second and high frequency clock to convert analog values on at least one analog input to a plurality of corresponding digital values, each in an associated SAR conversion cycle;

the step of storing operable to store a representation of the resultant digital values; and

the step of processing operable to process the representation of the resultant digital values.

16. (Previously Presented): The method of Claim 15, wherein the step of storing is operable to store each of the resultant digital values separately.

17. (Previously Presented): The method of Claim 15, wherein the step of storing is operable to store an accumulated digital value of the resultant digital values as a single value.

18. (Previously Presented): The method of Claim 17, wherein the resultant digital values are all related to a single analog input.

19. (Previously Presented): The method of Claim 18, wherein the step of processing by the digital processing section is operable to determine the average of the accumulated digital value.

20. (Currently Amended): The method of Claim 15, where there are provided a plurality of analog inputs, each operable to receive a separate analog signal, and further comprising the step of selecting with a multiplexer select ones of the analog inputs for interface with the SAR ADC ~~converter~~ for each of the data conversion operations carried out thereby in response to the generation of the convert request.

21. (Previously Presented): The method of Claim 15, wherein all of the data conversion operations are completed within at least one cycle of the low frequency clock.

22. (Previously Presented): A processing system including a SAR analog-to-digital converter (ADC), comprising:

a low frequency clock and a high frequency clock;

a sampling device for tracking an analog input voltage during a tracking phase to sample the value thereof;

a conversion engine operable to initiate a conversion cycle referenced to an edge of the low frequency clock;

said conversion engine converting the sampled data in a conversion operation during a data conversion cycle, which conversion operation requires a plurality of conversion clock cycles; and

a timing engine for controlling the timing of at least a portion of the conversion operation during the data conversion cycle utilizing the high frequency clock as the conversion clock.

23. (Previously Presented): The system of Claim 22, wherein said timing engine is operable to utilize said high frequency clock during the conversion cycle to control the timing of the at least a portion of the conversion operation proximate in time to said conversion engine initiating the conversion cycle.

24. (Previously Presented): The system of Claim 22, wherein the at least a portion of the conversion operation comprises substantially all of the conversion operation.

25. (Previously Presented): The processing system of Claim 25, wherein the SAR ADC has an n-bit resolution and said conversion engine includes:

a bit tester for testing each of the n-bits during the conversion operation to determine the logic state thereof, the timing thereof determined by a conversion clock that generates the conversion clock cycles;

a conversion clock for generating the conversion clock from the low frequency clock during the tracking phase; and

said timing engine operable to generate the conversion clock from said high frequency clock for the at least a portion of the conversion operation.

26. (Previously Presented): The processing system of Claim 25, wherein said timing engine is operable to generate said conversion clock substantially only during the at least a portion of the conversion operation.

27. (Previously Presented): The processing system of Claim 25, wherein the at least a portion of the conversion operation does not include the time to test all of the n-bits.

28. (Previously Presented): The processing system of Claim 25, wherein the at least a portion of the conversion operation includes the time to test substantially all of the n-bits.

29. (Previously Presented): The processing system of Claim 25, wherein the at least a portion includes all of the n-bits.

30. (Previously Presented): The processing system of Claim 22, wherein said conversion engine is operable to initiate said conversion operation in response to the generation of a convert initiation signal generated by a processing unit.

31. (Previously Presented): The processing system of Claim 30, wherein said processing unit operates from said low frequency clock and, during controlling the timing of at least a portion of the conversion operation by said timing engine, said processing unit continues to operate on said low frequency clock.

32. (Previously Presented): The processing system of Claim 22, wherein the SAR ADC operates in a power up mode and in a power down mode, when in the power down mode, said conversion engine operable to:

operate the SAR ADC in a low power mode;

receive a power up signal and, in response thereto:

apply power to the SAR ADC,

initiate the tracking operation,

delay the start of the conversion cycle by a predetermined delay to allow the SAR ADC to stabilize, and

after the end of the conversion cycle, remove power to the SAR ADC.

33. (Previously Presented): The processing system of Claim 32, and further comprising a delay block for introducing a known programmable amount of delay to force the tracking operation to continue for that programmable amount of delay and delaying the start of the conversion cycle for the programmable amount of delay.

34. (Currently Amended): A mixed signal processing system for controlling the operation of a SAR ADC, comprising:

a digital processing section;

a first and low frequency clock for operating said digital processing section;

a second and high frequency clock that has a clock frequency that is higher than the frequency of said low frequency clock;

said digital processing section generating a convert request to instruct the SAR ADC to initiate a conversion operation;

a conversion engine for, in response to the generation of the convert request, operating the SAR ADC in a data conversion operation on said second and high frequency clock to convert an analog value on an analog input to a digital value in a SAR conversion cycle;

a memory for storing the resultant digital value for processing by said digital processing section; and

after storage of the resultant digital value in said memory, said digital processing section processing the resultant digital value.

35. (Currently Amended): The processing system of Claim 34, wherein the conversion operation is completed within at least a single cycle of the said low frequency clock.

36. (Currently Amended): The processing system of Claim 34, wherein:

said conversion engine, in response to the generation of the convert request, operating the SAR ADC in a plurality of data conversion operations on said second and high frequency clock to convert analog values on at least one analog input to a plurality of corresponding digital values, each in an associated SAR conversion cycle;

said memory operable to store a representation of the resultant digital values; and

said ~~Said~~ digital processing section operable to process the representation of the resultant digital values.

37. (Previously Presented): The processing system of Claim 36, wherein said memory is operable to store each of the resultant digital values separately.

38. (Previously Presented): The processing system of Claim 36, wherein said memory is operable to store an accumulated digital value of the resultant digital values as a single value.

39. (Previously Presented): The processing system of Claim 38, wherein the resultant digital values are all related to a single analog input.

40. (Previously Presented): The processing system of Claim 39 wherein said digital processing section is operable to determine the average of the accumulated digital value.

41. (Currently Amended): The processing system of Claim 36, where there are provided a plurality of analog inputs, each operable to receive a separate analog signal, and further comprising a multiplexer for selecting select ones of the analog inputs for interface with the SAR ADC ~~converter~~ for each of the data conversion operations carried out by said conversion engine in response to the generation of the convert request by said digital processing section.

42. (Previously Presented): The processing system of Claim 36, wherein all of the data conversion operations are completed within at least one cycle of the low frequency clock.